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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/751,377	12/29/2000	. Anthony X. Jarvis	00-BN-055 (STMI01-00055)	8283	
30425 75	590 08/03/2004	•	EXAM	IINER	
STMICROELECTRONICS, INC.			O BRIEN	O BRIEN, BARRY J	
MAIL STATIO	N 2346	•			
1310 ELECTRONICS DRIVE			ART UNIT	PAPER NUMBER	
CARROLLTON, TX 75006			2183		
			DATE MAILED: 08/03/200	DATE MAILED: 08/03/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)				
Advisory Action	09/751,377	JARVIS, ANTHONY X.				
Advisory Action	Examiner	Art Unit				
	Barry J. O'Brien	2183				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address						
THE REPLY FILED 29 June 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.						
PERIOD FOR REPLY [check either a) or b)]						
a) The period for reply expires 3 months from the mailing date of the final rejection. b) The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).						
Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
1. A Notice of Appeal was filed on Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.						
2. The proposed amendment(s) will not be entered because:						
(a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);						
(b) they raise the issue of new matter (see Note below);						
(c) \boxtimes they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or						
(d) They present additional claims without canceling a corresponding number of finally rejected claims.						
NOTE:						
3. Applicant's reply has overcome the following rejection(s):						
4. Newly proposed or amended claim(s) would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).						
5. ☐ The a) ☐ affidavit, b) ☐ exhibit, or c) ☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.						
6. The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.						
7.⊠ For purposes of Appeal, the proposed amendment(s) a)⊠ will not be entered or b)□ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.						
The status of the claim(s) is (or will be) as follows:						
Claim(s) allowed: none.						
Claim(s) objected to: <u>none</u> .						
Claim(s) rejected: <u>1-4,6-14 and 16-22</u> .						
Claim(s) withdrawn from consideration: <u>none</u> .						
8. The drawing correction filed on is a) approved or b) disapproved by the Examiner.						
9. Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s).						
10. Other:						
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U.S. Patent and Trademark Office PTOL-303 (Rev. 11-03) Continuation of 5. does NOT place the application in condition for allowance because: The Applicants amendment filed on 6/29/04 argues that the prior art reference Nakanishi, U.S. Patent No. 5,805,852, has not taught all of the limitations of claim 1, specifically both a plurality of tristate line drivers with outputs connected to a common read data channel and a multiplexer with an input connected to the common read data channel (see p.13-14 of the present amendment). However, Nakanishi has taught the above limitations. While a multiplexer has not been explicitly taught by Nakanishi, the functionality of a multiplexer has been taught by Nakanishi to be comprised within the tristate bypass network of Fig.3 (see Col.6 lines 5-23 and Col.11 lines 16-31). Furthermore, Nakanishi has taught how the same tristate bypass network of Fig.3 encompasses the functionality of the multiplexers in the prior art that were used for selecting between multiple bypass values (see Fig.28 and Col.3 lines 39-53). Therefore, the tristate bypass network of Nakanishi functions as both a multiplexer and bypass circuitry. Furthermore, the claim language has only limited the first plurality of tristate output channels to be "coupled" to the common read data channel, and the first multiplexer to be similarly "coupled' to the common read data channel. Because any data value from the register file or from any of the results buffers can be input back into any latch (see Col.10 lines 11-67), any of the buses 1-1 to 4-2 of Fig.3 can be considered a "common read data channel", and thus both the outputs of any of the plurality of tristate buffers and the input of the multiplexer of Fig.3 are "coupled" to a "common read data channel".

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